Simon Fraser University

Mechatronic Systems Engineering

Midterm Exam for
ENSC 331: Introduction to MEMS

Instructor: Behraad Bahreyni

28 June 2010

Time: 105 minutes

Name: Solutions

Student number:________________

Question	Mark
1	/ 26
2	/ 10
3	/ 18
4	/ 10
5	/ 16
6	/ 20
Total:	/ 100

Deal-Groove model for oxidation rate of silicon:	$t_{ox}^2 + At_{ox} = B(t+\tau)$

Deal-Groove rate constants for oxidation of *bare* (111) silicon wafers

	A (μm)		*B (μm²/hr)*	
Temperature (°C)	**Dry**	**Wet**	**Dry**	**Wet**
800	0.512	2.18	0.0013	0.084
900	0.252	0.676	0.0040	0.172
1000	0.138	0.252	0.0104	0.316
1100	0.083	0.109	0.0236	0.530
1200	0.053	0.052	0.0479	0.828

Doping profiles and surface density of dopants (*x* is the depth into the wafer):

Diffusion with *constant concentration* of dopants at the surface	$C(x,t) = C_s\, erfc\left(\frac{x}{2\sqrt{Dt}}\right)$	$Q = \frac{2\sqrt{Dt}}{\sqrt{\pi}} C_s$
Diffusion with *constant number* of dopants at the surface	$C(x,t) = \frac{Q}{\sqrt{\pi D t}} \exp\left(-\frac{x^2}{4Dt}\right)$	Q
Doping with implantation	$C(x) = C_p\, \exp\left(-\frac{(x-R_P)^2}{2\Delta R_P^2}\right)$	$Q = \sqrt{2\pi}\, C_P \Delta R_P$

Mean free path of gas molecules	$\lambda = \frac{k_B T}{\sqrt{2}\sigma P}$

Thickness of spun photoresist	$T = K\frac{C\,\eta}{\sqrt{\omega}}$

Resolution in proximity and contact printing	$R = \frac{3}{2}\sqrt{\lambda\left(s+\frac{z}{2}\right)}$

Angle between $\langle h_1k_1l_1 \rangle$ and $\langle h_2k_2l_2 \rangle$ directions	$\cos\theta = \frac{h_1h_2 + k_1k_2 + l_1l_2}{\sqrt{(h_1^2+k_1^2+l_1^2)(h_2^2+k_2^2+l_2^2)}}$

Diffusion constant	$D = D_0 \exp\left(-\frac{E_a}{k_B T}\right)$

Boltzmann constant $k_B = 1.38 \times 10^{-23}\, J/K$	$1eV = 1.6 \times 10^{-19}\, J$
1 atmosphere = 760 Torr = 101 325 Pa	$1\mu m = 1000nm = 10^{-4}cm$

Question 1 (5+5+8+8 marks)

1-I. What is NOT an advantage of e-beam lithography systems over typical UV lithography?

(a) No need for a mask (b) Large depth of focus

(c) Speed of operation (d) Better resolution

(e) None of the above

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1-II. What are the miller indices for the plane shown here?

(a) $(2, \bar{4}, \infty)$ (b) $(\bar{4}, 2, 0)$

(c) $(2, \bar{4}, 0)$ (d) $(2, \bar{1}, 0)$

(e) None of the above

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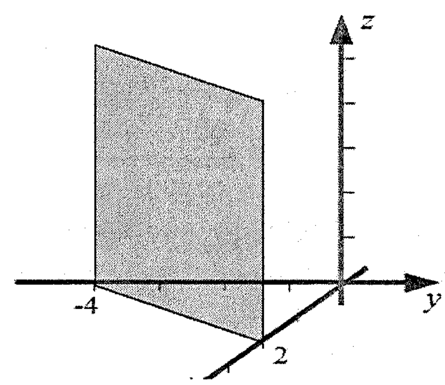

1-III. List four points that a process engineer should bear in mind when designing a microfabrication process flow. Do NOT write more than 4.

a) Thermal budget 2

b) Chemical compatibility 2

c) Mechanical stability 2

d) Material property control 2

Process accuracy

Cross-contamination

1-IV. We want to compare thermal evaporation and basic sputtering methods for deposition of a 500nm layer of aluminum. Which technique:

a) Has a higher deposition rate? Evaporation 2

b) Results in more pure films? Evaporation 2

c) Is more conformal (i.e., covers surfaces more uniformly)? Sputtering 2

d) Is more suitable for a lift-off process? Evaporation 2

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Question 2 (6+4 marks):

We are implementing a modified version of the PolyMuMPS process where the oxide films are sputtered. The following layers are deposited and patterned one after the other:

a) 600nm of silicon nitride (CVD)
b) 500nm of polysilicon (CVD+RIE)
c) 2μm of silicon dioxide (Sputtering+RIE)
d) 2μm of polysilicon (CVD+RIE)
e) 750nm of silicon dioxide (Sputtering+RIE)
f) 1.5μm of polysilicon (CVD+RIE)
g) 500nm of gold (Lift-off)

2-I- Starting with the first layer on the substrate, what layers will be present on the BACKSIDE of the wafer after the process is completed?

1. 600 nm of SiN (1.5)
2. 500 nm of Poly (1.5)
3. 2 μm of Poly (1.5)
4. 1.5 μm of Poly (1.5)
5. ______
6. ______
7. ______
8. ______
9. ______
10. ______

Each wrong extra layer (−1)

2-II- If a corner of the design is empty from the top side (i.e., all the structural layers are removed), what is the total thickness of the wafer at that point? Assume that the bare wafers are 400μm thick.

Wafer thickness: 405.2 μm

600nm (SiN) + 400μm (Si) + 600nm (SiN) + 4μm (Poly)

top (2) bottom (4)

Thickness 405.2 μm

Question 3 (6+12 marks)

3-I. A bare (111) silicon wafer was put inside a furnace for dry oxidation for 2 hours at 1000°C. What is the thickness of the oxide grown on the surface of the wafer?

$t_{ox} =$ 91 nm

$A = 0.138$, $B = 0.0104$, $\tau = 0$ (2)

$$t_{ox}^2 + 0.138\, t_{ox} - 0.0104 \times 2 = 0$$

$$\Rightarrow t_{ox} = \frac{-0.138 \pm \sqrt{0.138^2 + 4 \times 2 \times 0.0104}}{2}$$

$t_{ox} = 0.091\, \mu m$ (4)

3-II. After 2 hours, we introduce steam into the furnace and continue to grow a wet oxide for another ~~2~~ hour~~s~~. What is the OVERALL thickness of the oxide layer?

$t_{ox} =$ 477 nm

$A = 0.252$, $B = 0.316$

$$\tau = \frac{0.091^2 + 0.252 \times 0.091}{0.316} = 0.099\ hr$$ (6)

$$t_{ox}^2 + 0.252\, t_{ox} - 0.316\,(1 + 0.099) = 0$$

$$\Rightarrow t_{ox} = \frac{-0.252 \pm \sqrt{0.252^2 + 4 \times 0.316\,(1.099)}}{2}$$

$\Rightarrow t_{ox} = 0.477\, \mu m$ (6)

Question 4 (10 marks)

The background dopant concentration on an n-type wafer is 10^{17} atoms/cm^3. We dope the wafer using a fixed number of boron atoms at the surface. What is the required density of boron atoms at the surface of the wafer (in atoms/cm^2) so that the a pn junction is formed at a depth of 350nm after putting the wafer inside a furnace at 1000°C for 30 minutes?

For boron, $E_a = 3.46eV$ and $D_0 = 0.76\ cm^2/s$.

$Q =$ 4.9×10^{16} $atoms/cm^2$

$T = 1000 + 273 = 1273$ → (3)

$$D = 0.76 \times e^{\frac{-3.46 \times 1.6 \times 10^{-19}}{1.38 \times 10^{-23} \times 1273}} = 1.6 \times 10^{-14}\ cm^2/s$$

$$C(x,t) = \frac{Q}{\sqrt{\pi D t}} \exp\left(\frac{-x^2}{4Dt}\right) \quad (2)$$

$Dt = 2.82 \times 10^{-11}\ cm^2$

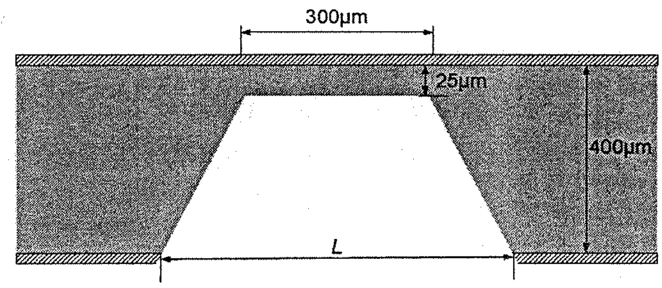
$x = 0.35 \times 10^{-4}\ cm$

$\Rightarrow C(0.35 \times 10^{-4}, 1800) = 10^{17}$ (2)

$\Rightarrow Q = 4.9 \times 10^{16}$ atoms/cm^2 (3)

Question 5 (6+10 marks)

We would like to fabricate a square diaphragm on a (100) wafer that is 25μm thick (cross section shown to the right). We etch the wafer inside a KOH solution from the backside using a masking layer of thermally grown SiO_2. The relative etch rate of (100) to (111) planes is 100:1. The relative etch rate of (100) planes to SiO_2 is 150:1. The sides of the diaphragm are aligned with <100> direction.



6-I. What is the minimum required thickness of the SiO_2 layer so that it survives the process?

SiO_2 *thickness*: 2.5 μm

Etched silicon = 400 − 25 = 375 μm (2)

Amount of SiO_2 = $\frac{375}{150}$ = 2.5 μm (4)

6-II. What is the length of the side of the mask opening (L) on the backside of the wafer?

Side length: 830.33 μm

Angle between (111) & (100) planes

$\cos\theta = \frac{1}{\sqrt{3}} \rightarrow \theta = 54.7°$ (4)

Mask opening = $300 + 2 \times \frac{375}{\tan 54.7} = 830.33 \mu m$ (2) (4)

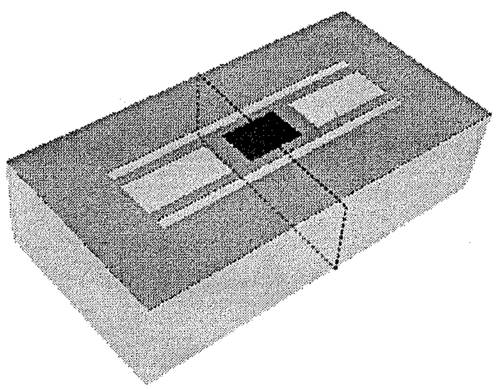
More exact:

830.33 − Amount etched in <111> direction

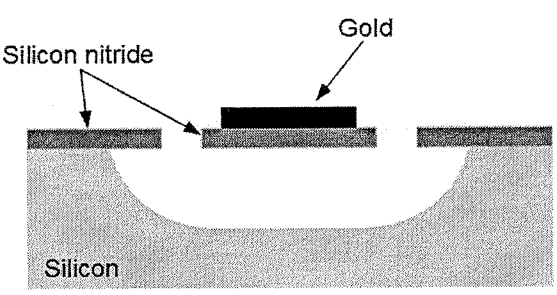
$= 830.33 - 2 \times \frac{375/100}{\sin 54.7} = 821.14$

Question 6 (20 marks)

We want to fabricate the structure shown to the right on a bare silicon wafer using the processing steps that are available to us as listed below. Design a process flow based on these processes to fabricate the device.



- Positive resist spinning
- UV Lithography
- Positive resist developing
- Positive resist stripping
- Thermal oxidation
- Thermal evaporation
- Piranha cleaning
- Nitride etching
- Nitride CVD
- HNA etching
- KOH etching
- XeF_2 etching
- Silicon RIE



Write down the processing steps for your fabrication flow. You do not need to provide details on chemistry, etch rate, etc. Use as few steps as needed for a reliable process.

Number of masks: 2 (2)

Step 1: Piranha Clean

Step 2: Nitride CVD

Step 3: Resist Spinning — Each extra step (−1)

Step 4: UV Litho (Mask 1) — Each missing Step (−2)

Step 5: Resist developing

Step 6: Nitride etch

Step 7: Piranha Clean / Resist stripping

Step 8: Resist spinning

Step 9: UV Litho (Mask 2)

Step 10: Resist Developing

Step 11: Gold evaporation

Step 12: Resist stripping

Step 13: XeF_2 etch

Step 14:

Step 15:

Step 16:

Step 17:

Step 18:

You can use this space to answer the question or for your calculations
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